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10/676,116	10/02/2003	Seong Woon Kim	123056-05004412	6033

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EXAMINER	
STIGLIC, RYAN M	

ART UNIT	PAPER NUMBER
2111	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/676,116	KIM ET AL.	
	Examiner	Art Unit	
	Ryan M. Stiglic	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 November 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 3-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1 and 3-9 are pending and have been examined.

2. Claims 1 and 3-9 are rejected.

Response to Arguments

3. Applicant's arguments filed November 7, 2007 have been fully considered but they are not persuasive. Applicant contends that Philbrick fails to disclose and/or fairly suggest "the TOE communicating with the MAC directly and not over the peripheral device bus..." (*see page 5 of the remarks*) with regards to Figures 1 and 8. Philbrick teaches an alternative embodiment in Figures 24-25 where the network storage apparatus is suggested to have a TOE (*Sequencer block 732 and Processor 470 [referenced as 780 in the disclosure] act as a TOE since together they perform the functions of a TOE as claimed.*) communicating with a MAC (*Fig. 24, 722*) directly and not over the peripheral device bus (*Figure 24 shows the MAC connected to the sequencer, through signal line 410 and then processor 470 [780] through queue manager 2103.*). In light of the teachings of Philbrick (Fig. 24), applicant's arguments are not persuasive.

Applicant has further amended claim 1 to include limitations from claim 8 and alleges "Philbrick fails to disclose at least the sequential arrangement of the PCI bridge, the TOE and the MAC, as well as the DSB, recited in amended claim 1" (*see page 6*). Applicant's arguments are not persuasive for the reasons listed above and for the reasons to be discussed below.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1 and 3-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent Application Publication No. 2001/0037406 (hereinafter Philbrick).

As previously suggested in the Final Office Action dated July 10, 2007, Philbrick discloses A network-storage apparatus (Fig. 1, 'INIC' 22; paragraph [0042]) for high-speed streaming data transmission through a network, the apparatus comprising: an internal peripheral device bus separated from a peripheral device bus outside the network-storage apparatus, for transmitting data between devices inside the network-storage apparatus (Fig. 1, 48; [0043]); a peripheral device bus bridge for transferring bus transaction from a host processor to the internal peripheral device bus and transferring bus transaction for a host processor executing inside the network-storage apparatus or a main memory to a bus bridge (Fig. 1, 50; [0043]); a disk controller for controlling a plurality of disc storage connected to the network-storage apparatus and managing reading and writing data from and to the disc storage (Fig. 1, 72; [0045]); a peripheral memory for storing transmitted data between the disc storage and the network (Fig. 1, 46; [0043]); a peripheral memory controller for controlling the peripheral memory and storing or outputting the transmitted data between the disc storage and the network ([0053]; and a TOE for reading data to be transmitted to the network from the peripheral memory, constructing the data in the form of

a packet including information for network transmission ([0089] discloses a situation where a client on the network requests data stored in a peripheral memory of the server and the INIC gathers the information and sends the data packets to the client with prepended headers "it created based on the server CCB"), transmitting the packet to the network, and storing the data received from the network in the peripheral memory through the peripheral memory controller (Fig. 1, items 52,58,60; [0043-0062]); wherein the network storage apparatus stores the streaming data received through network on the disk storage in the form of zero copy and transmits the streaming data stored on the disk through the network in the form of zero copy, between the plurality of disk storage of an internet server computer system and a network (see section 4 from the Office Action dated September 18, 2006; also see Philbrick [0045, 0053, 0011-0013, 0087-0089]), wherein the peripheral device bus is a PCI bus and the peripheral device bus bridge roles a PCI bridge ([0066]). While Philbrick discloses (Fig. 1) a MAC and TOE, figure 1 fails to teach the TOE communicating with the MAC directly and not over the peripheral device bus.

Philbrick teaches an alternative embodiment in Figures 24-25 where the network storage apparatus is suggested to have a TOE (*Sequencer block 732 and Processor 470 [referenced as 780 in the disclosure] act as a TOE since together they perform the functions of a TOE as claimed.*) communicating with a MAC (*Fig. 24, 722*) directly and not over the peripheral device bus (*Figure 24 shows the MAC connected to the sequencer, through signal line 410 and then processor 470 [780] through queue manager 2103.*).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to incorporate the teachings of Figures 24-25 into Figure 1 such that the MAC, TOE and peripheral bridge are provided in a single ASIC thus saving power consumption while increasing performance.

For claim 1 Philbrick teaches:

A network-storage apparatus (Fig. 1, 'INIC' 22; paragraph [0042]) for high-speed streaming data transmission through a network, the apparatus comprising:

- an internal peripheral device bus separated from a peripheral device bus outside the network-storage apparatus, for transmitting data between devices inside the network-storage apparatus (Fig. 1, 48; [0043]);
- a peripheral device bus bridge for transferring bus transaction from a host processor to the internal peripheral device bus and transferring bus transaction for a host processor executing inside the network-storage apparatus or a main memory to a bus bridge (Fig. 1, 50; [0043]);
- a disk controller for controlling a plurality of disc storage connected to the network-storage apparatus and managing reading and writing data from and to the disc storage (Fig. 1, 72; [0045]);
- a peripheral memory for storing transmitted data between the disc storage and the network (Fig. 1, 46; [0043]);
- a peripheral memory controller for controlling the peripheral memory and storing or outputting the transmitted data between the disc storage and the network ([0053]; and

- a TCP/IP offload engine (TOE) (Fig. 24, combination of sequencers 732 and Proc 470/780) for reading data to be transmitted to the network from the peripheral memory, constructing the data in the form of a packet including information for network transmission ([0089] discloses a situation where a client on the network requests data stored in a peripheral memory of the server and the INIC gathers the information and sends the data packets to the client with prepended headers "it created based on the server CCB"), transmitting the packet to the network, and storing the data received from the network in the peripheral memory through the peripheral memory controller ([0043-0062]; also see paragraphs [0132-0152] for a more detailed explanation of the TOE operation); and
- a media access control unit MAC situated between the TOE and the network (Fig. 24, 722; [0132]);
- wherein the network storage apparatus stores the streaming data received through network on the disk storage in the form of zero copy and transmits the streaming data stored on the disk through the network in the form of zero copy, between the plurality of disk storage of an internet server computer system and a network (see section 4 from the Office Action dated September 18, 2006; also see Philbrick [0045, 0053, 0011-0013, 0087-0089]), wherein the peripheral device bus is a PCI bus and the peripheral device bus bridge roles a PCI bridge ([0066]) ;
- wherein the TOE is situated between the peripheral device bus and the MAC such that streaming data to and from the network passes the MAC and the TOE to the peripheral device bus, the TOE communicating with the MAC directly and not over the peripheral

device bus which is shared with the disk controller and peripheral memory controller, thereby enabling high-speed streaming data through the network (The incorporation of the teachings of figures 24 and 25 into figure 1 of Philbrick yields a similar structure to that of figure 1 except that the MAC [fig 24, 722] and TOE [Fig. 24, items 732 and 470.780] are provided in serial ordering without the intervening peripheral device bus [0132]. The peripheral device bus is however connected after the TOE [Fig. 24, 756 is a peripheral device bus connection.]. Therefore the combination of figures 1 and 24/25 yields an INIC 22 having an ASIC comprising a MAC and TOE sequentially which then interface the peripheral device bus 48.); and

- wherein the TOE includes a DSB table having information on packet data to be transferred to disk storage immediately among data packets received from the network ([0043-0062]; A communication control block (CCB) stores information on packet data to be transferred to/from disk storage immediately [e.g. "fast-path processing"].).

For claim 3, Philbrick teaches:

The apparatus of claim 1, wherein the disk controller is connected to a plurality of disc storages in parallel through a disk interface bus and accesses to the data in a pipeline manner ([0111-0113]).

For claim 4, Philbrick teaches:

The apparatus of claim 1, wherein the disk controller reads and writes data from and to a plurality of disc storages in a stripping manner ([0044-0045] Where stripping is a form of RAID clearly covered by the scope of the word RAID).

For claim 5, Philbrick teaches:

The apparatus of claim 1, wherein the peripheral memory controller constructs a memory table so as to cache data transmitted from and to the network ([0045-0046,0055,0059-0060,0110] etc.).

For claim 6, Philbrick teaches:

The apparatus of claim 1, wherein the peripheral memory controller is provided a register for indicating size of the peripheral memory inside the peripheral memory controller, and transmits a great deal of data in a DMA manner ([0110,0052-0053]).

For claim 7, Philbrick teaches:

The apparatus of claim 1, wherein the peripheral memory controller deletes contents of a memory table thereof when finishing accessing to the peripheral memory ([0045-0046,0055,0059-0060,0110]).

For claim 8, Philbrick teaches:

The apparatus of claim 1, wherein the TOE is configured to transmit a data packet received from the network to the peripheral memory to store the data packet if the data packet storable in the

disk storage has information matching DSB, and transmitting a data packet to a general network stack otherwise (See paragraphs [0043-0062] for an overview of "fast-path processing".).

For claim 9, Philbrick teaches:

The apparatus of claim 1, wherein the TOE reads data to be transmitted to the network from the peripheral memory, constructs the data in the form of a packet and transfers the data packet to the network when the data to be transmitted is stored in the peripheral memory and the TOE receives a data transmission instruction from a host processor ([0043-0062]).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ryan M. Stiglic whose telephone number is 571.272.3641. The examiner can normally be reached on Monday - Friday (6:00-3:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 571.272.3632. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

RMS

Paul R. Myers

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PRIMARY EXAMINER